

1. A Chip Scale Package (CSP) comprising:

3 providing a silicon chip having I/O pads;

an under-ball metallurgy (UBM) layer on the surface of said
6 I/O pads;

a substrate with an adhesive (adsubstrate), and having
9 openings corresponding to the locations of said I/O pads;
and

12 ball mountings formed over said adsubstrate and reaching
said UBM layer over said I/O pads on said chip.

2. The CSP of claim 1, wherein said first layer of I/O pads
comprise aluminum alloy or copper.

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3. The method of claim 1, wherein said UBM layer comprises
nickel or copper.

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4. The CSP of claim 1, wherein said substrate comprises
bismaleimide triazine (BT).

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5. The CSP of claim 1, wherein said substrate comprises Ball Grid Array (BGA).

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6. The CSP of claim 1, wherein said substrate has a thickness between about 150 to 300 μm , and wherein said adhesive has a thickness between about 10 to 100 μm .

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7. The CSP of claim 1, wherein said ball mountings comprise tin-lead or tin-silver alloy.

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8. The CSP of claim 1, wherein said ball mountings have a height between about 300 to 800 μm .

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9. The CSP of claim 1, wherein said I/O pads are area array (AA) type, or redistributed to a redistribution layer to form AA pads.

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10. The CSP of claim 1, wherein said CSP is encapsulated in a molding material comprising epoxy resin.

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11. A method of forming a chip scale package (CSP) comprising the steps of:

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providing one or more chips having I/O pads with UBM layer on the surface of said I/O pads;

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providing a substrate;

9 applying an adhesive layer over said substrate, thus forming an adsubstrate composite;

12 forming openings in said adsubstrate composite to match the spacing of corresponding said I/O pads of said chip;

15 attaching said chip(s) on said adsubstrate composite wherein said I/O pads of said chip(s) are placed on the corresponding openings on said adsubstrate composite to form

18 a package;

forming a molding material around said package;

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performing ball mounting over said openings on said adsubstrate of said package; and

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forming said CSP.

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12. The method of claim 11, wherein said chip comprises silicon.

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13. The method of claim 11, wherein said I/O pads are area array (AA) type, or are redistributed to a redistribution layer to form AA I/O pads.

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14. The method of claim 11, wherein said substrate comprises bismaleimide triazine (BT).

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15. The method of claim 11, wherein said substrate comprises Ball Grid Array (BGA).

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16. The method of claim 11, wherein said substrate has a thickness between about 150 to 300 μm .

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17. The method of claim 11, wherein said adhesive layer comprises polyimide thermocompression adhesive.

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18. The method of claim 11, wherein said adhesive layer has a thickness between about 10 to 100 μm .

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19. The method of claim 11, wherein said forming said openings is accomplished by mechanical or laser drilling, or screen printing.

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20. The method of claim 11, wherein said openings have a diameter between about 350 to 900 μm .

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21. The method of claim 11, wherein said attaching said chip(s) is accomplished by subjecting said adsubstrate to a temperature between about 250 to 350 $^{\circ}\text{C}$ at a pressure between about 1.5 to 2.5 Mpascals.

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22. The method of claim 11, wherein said molding material comprises epoxy resin.

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23. The method of claim 11, wherein said molding material has a thickness between about 100 to 500 μm .

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24. The method of claim 11, wherein said performing said ball mounting is accomplished with a solder comprising tin-lead or tin-silver alloy.

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25. The method of claim 11, wherein said ball mountings have a height between about 300 to 800 μm .

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26. A method of forming a chip scale package (CSP) comprising the steps of:

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providing a wafer having a plurality of chip sites with I/O pads;

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forming an under-ball metal (UBM) layer over said I/O pads;

9 forming an adhesive layer over said UBM layer on said wafer to form an adwafer;

12 forming openings in said adhesive layer on said adwafer to reach said I/O pads underlying said UBM layer;

15 die sawing said adwafer to form said chip scale package (CSP);

18 providing a substrate having openings corresponding to said I/O pads;

21 attaching said CSP with said adhesive to said substrate; and

forming ball mountings on said openings on said substrate to

24 attach to said I/O pads on said CSP.

27. The method of claim 26, wherein said wafer comprises silicon.

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28. The method of claim 26, wherein said I/O pads comprise aluminum alloy or copper.

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29. The method of claim 26, wherein said I/O pads are area array (AA) type, or redistributed to a redistribution layer

3 to form AA pads.

30. The method of claim 26, wherein said UBM layer comprises nickel and/or copper.

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31. The method of claim 26, wherein said forming said adhesive layer over said UBM layer comprises lamination,

3 spin coating or screen printing.

32. The method of claim 26, wherein said adhesive layer comprises thermocompression polyimide adhesive.

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33. The method of claim 26, wherein said adhesive layer has a thickness between about 10 to 100 μm .

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34. The method of claim 26, wherein said forming said openings comprise laser drilling, photolithography, or silk

3 screening.

35. The method of claim 26, wherein said openings have a diameter between about 250 to 750 μm .

36. The method of claim 26, wherein said substrate comprises bismaleimide triazine (BT) having a thickness between about 150 to 300 μm .

37. The method of claim 26, wherein said substrate comprises Ball Grid Array (BGA).

38. The method of claim 26, wherein said attaching said BGA substrate to said adhesive layer is accomplished at a temperature between about 250 to 350 $^{\circ}\text{C}$, and pressure between about 1.5 to 2.5 Mpascals.

39. The method of claim 26, wherein said ball mountings comprise solder having a composition lead-tin or tin-silver.

40. The method of claim 26, wherein said mounting balls have a height between about 300 to 800 μm .

41. The method of claim 26, wherein said CSP is encapsulated in a molding material comprising epoxy resin.